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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BERNSTEIN, ALLISON	

ART UNIT	PAPER NUMBER
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,061	LUK ET AL.	
	Examiner	Art Unit	
	Allison P. Bernstein	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2007 and 22 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33,54,55 and 58* is/are pending in the application.

4a) Of the above claim(s) *11-33,54 and 55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request For Continued Examination, filed 27 July 2007.

Acknowledgment is made of applicant's amendment, filed on 24 July 2007 and 22 August 2007. The changes and remarks disclosed therein have been considered.

Claims 1-33, 54, 55, and 58 are pending in the application. Claims 11-33, 54, and 55 are withdrawn from further consideration. Claim 1 is currently amended. Claim 1 is an independent claim.

Election/Restrictions

In response to Applicant's arguments regarding the restriction requirement, the examiner agrees that if claim 1 is eventually allowed in its present form, or if claim 1 is subsequently amended but yet remains generic to all or some of such dependent claims, the examiner will maintain some of all of the withdrawn claims, as appropriate.

Also note that when two or more species are claimed, a requirement to a single species may be proper if the species are mutually exclusive. The mutually exclusive characteristics identified in the restriction requirement dated 16 October 2006 make the search burdensome.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-10** are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu (US 2003/0147277).

3. **Regarding claim 1,** Hsu discloses, in figure 4, a gated diode memory cell comprising: at least one transistor (for example 210) having a diffusion region; and a gated diode (for example 220) having a first terminal connected to the diffusion region of the at least one transistor (through capacitance connection through the gate of the transistor) and a second terminal connected to a wordline (for example WL_0).

4. **Regarding claim 2,** Hsu discloses, in figure 4, a gated diode memory cell as defined in Claim 1 wherein the first terminal of the gated diode (for example 220) forms one terminal of a storage cell and the second terminal of the gated diode (for example 220) forms another terminal of the storage cell [0033].

5. **Regarding claim 3,** Hsu discloses, in figures 4 and 9A-9D, a gated diode memory cell as defined in Claim 2 wherein the first terminal is a gate (for example 906A

in figure 9D) of the gated diode (for example 220), wherein the gate is implemented in the form of a shallow trench (see also abstract and [0064]).

6. **Regarding claim 4,** Hsu discloses, in figures 4 and 9A-9D, a gated diode memory cell as defined in Claim 3, wherein the gate (for example 906A in figure 9D) of the gated diode (for example 220) comprises a poly trench (906A in figure 9D) surrounded by thin oxide (905B) with silicon (for example 913) disposed underneath and surrounding the thin oxide (905B) (see also [0069]).

7. **Regarding claim 5,** Hsu discloses, in figures 4 and 9A-9D, a gated diode memory cell as defined in Claim 4 wherein the poly trench (906A) is cylindrical (see figures 9A-9D).

8. **Regarding claim 6,** Hsu discloses, in figures 4 and 9A-9D, a gated diode memory cell as defined in claim 4 wherein the gate (for example 906A in figure 9D) of the gated diode (for example 220) comprises a metal oxide semiconductor ("MOS") capacitor ([0064] and [0033]).

9. **Regarding claim 7,** Hsu discloses, in figures 4 and 3A-3B, a gated diode memory cell as defined in Claim 2 wherein the gate (216) of the gated diode (for example 220) is planar (see figure 3A).

10. **Regarding claim 8,** Hsu discloses, in figures 4 and 3A-3B, a gated diode memory cell as defined in Claim 7 wherein the gate (216) of the gated diode (for example 220) is disposed above a diffusion area (below 215 in figure 3A).

11. **Regarding claim 9,** Hsu discloses, in figures 4 and 3A-3B, a gated diode memory cell as defined in Claim 8, further comprising an oxide layer (215) disposed between the gate (216) of the gated diode (220) and the diffusion area (below 215).

12. **Regarding claim 10,** Hsu discloses, in figures 4 and 3A-3B, a gated diode memory cell as defined in Claim 7, wherein the gated diode (220) comprises a planar metal oxide semiconductor ("MOS") capacitor [0033].

13. **Claims 1, 2, and 58** are rejected under 35 U.S.C. 102(b) as being anticipated by Houghton et al. (US 5,757,693) ("Houghton").

14. **Regarding claim 1,** Houghton discloses, in figure 1, a gated diode memory cell comprising: at least one transistor (for example Tw0) having a diffusion region; and a gated diode (for example Tr0) having a first terminal connected to the diffusion region of the at least one transistor and a second terminal connected to a wordline (for example WLR0).

15. **Regarding claim 2,** Houghton discloses, in figure 1, a gated diode memory cell as defined in Claim 1 wherein the first terminal of the gated diode (for example Tr0) forms one terminal of a storage cell and the second terminal of the gated diode (for example Tr0) forms another terminal of the storage cell.

16. **Regarding claim 58,** Houghton discloses, in figure 1, a gated diode memory cell as defined in claim 1 wherein the at least one transistor (for example Tw0) and gated diode (for example Tr0) are a same type of FET (see figure 1).

Response to Arguments

17. Applicant's arguments filed 24 July 2007 have been fully considered but they are not persuasive.

18. In response to Applicant's argument that Hsu does not disclose or suggest a gated diode having a first terminal connected to a diffusion region of a transistor and a second terminal connected to a wordline, Hsu discloses a gated diode having a first terminal connected to a diffusion region of a transistor (through the capacitance connection through the gate of the transistor) and a second terminal connected to a wordline.

Conclusion

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allison P. Bernstein whose telephone number is 571-

272-9011. The examiner can normally be reached on Monday-Thursday 7AM-6PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

APB

VAN THU NGUYEN
PRIMARY EXAMINER